

**U.S. Patent Application**

**I/O ARCHITECTURE FOR INTEGRATED CIRCUIT PACKAGE**

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## I/O ARCHITECTURE FOR INTEGRATED CIRCUIT PACKAGE

### BACKGROUND

System performance may be improved by increasing the quality of I/O signals transmitted between an integrated circuit die and associated receivers. The previously-  
5 proposed Decoupled I/O, Power delivery Hybrid (DIPH) architecture attempts to increase this quality by disposing I/O signal connections on the perimeter of a die and by disposing power connections on the interior of the die. The die may therefore receive power signals through pins and vias within a package holding the die, while I/O signals may be received through a cable connected to conductive elements disposed on an upper surface of the  
10 package that are in turn connected to the perimeter of the die.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cutaway side elevation of a system according to some embodiments.  
FIG. 2 is a top view of a package according to some embodiments.  
FIG. 3 is a bottom view of a package according to some embodiments.  
15 FIG. 4 is a cutaway view of a cable according to some embodiments.  
FIG. 5 is a side elevation of a system according to some embodiments.

### DETAILED DESCRIPTION

FIG. 1 is a side elevation of system 100 according to some embodiments. System 100 includes integrated circuit die 105. Integrated circuit die 105 may be fabricated using  
20 any suitable substrate material and fabrication technique and may provide any functions. In some embodiments, integrated circuit die 105 is a microprocessor chip having a silicon substrate.

Die 105 is electrically coupled to solder bumps 106, which are in turn coupled to an upper surface of package 110. Solder bumps 106 may comprise Controlled Collapse Chip Connect (C4) solder bumps, and may be coupled to a surface of die 105 that includes active devices in a “flip-chip” arrangement. Package 110 may comprise any ceramic, organic, 5 and/or other suitable material including an interface compatible with solder bumps 106. In some embodiments, package 110 is electrically coupled to die 105 via wirebonds in addition or as an alternative to solder bumps 106.

As shown, some of solder bumps 106 are coupled to conductive elements 111. In some embodiments, conductive elements 111 receive I/O signals from respective solder 10 bumps 106 to which they are coupled. Conductive elements 111 may be disposed above and/or flush with the upper surface of package 110. Conductive elements 111 may comprise any conductive structure for achieving an electrical connection with respective solder bumps 106, such as a copper pad with nickel and/or gold plating. Conductive elements 111 according to some embodiments are illustrated in FIG. 2, which is a top view of system 100 15 without die 105.

The upper surface of package 110 also includes fan-out areas 112. FIG. 2 shows fan-out areas 112 in some detail. In particular, FIG. 2 shows electrical couplings 113a and 113b within fan-out areas 112. Electrical couplings 113a electrically couple each of conductive elements 111 to a respective one of conductive elements 114. Accordingly, conductive 20 elements 114 may receive I/O signals from respective ones of conductive elements 111 to which they are coupled. Electrical couplings 113a may comprise copper microstriplines, and conductive elements 114 may comprise any suitable conductive connection element.

As shown in FIG. 2, a footprint of conductive elements 111 may be smaller than a footprint of conductive elements 114. Such an arrangement may facilitate the connection of 25 a connector to elements 114 due to the increase in spacing between conductive elements.

Electrical couplings 113b may also comprise microstriplines. Couplings 113b may be coupled to vias 115 that vertically traverse package 110. Vias 115 may in turn be electrically coupled to conductive elements 116 disposed on and/or flush with a lower

surface of package 110. FIG. 3 is a bottom view of package 110 showing conductive elements 116. Conductive elements 116 may receive I/O signals from respective ones of conductive elements 111 to which they are coupled through associated vias 115. For a given number of conductive elements 111, the routing of I/O signals to an upper and lower 5 surface of package 110 may allow the use of an I/O connection to package 110 that has a greater conductor pitch than previously usable.

Package 110 also includes pin-through holes 117 for coupling pins 118 to die 105. Pins 118 are interface elements for mounting system 100 to a socket on a motherboard or directly to a motherboard. Pins 118 carry power and ground signals to die 105 according to 10 some embodiments. Other interface elements such as solder bumps may be used in place of or in addition to pins 118. According to some embodiments, package 110 is a surface-mountable substrate such as an Organic Land Grid Array substrate that may be mounted directly on a motherboard or mounted on a pinned interposer which mates with a socket of a motherboard. Packaging systems other than those mentioned above may be used in 15 conjunction with some embodiments.

In some embodiments, pins 118 are disposed around the perimeter of recess 119 of package 110 as shown in FIG. 3. Land-side capacitors may be mounted in recess 119 to assist the functionality of die 105 and/or to reduce resonance between system 100 and a board to which system 100 is mounted.

20 Connector 120 may be mechanically coupled to package 110 using any suitable currently or hereafter-known system. Connector 120 includes coupling surface 121 and coupling surface 122, which face one another. Coupling surface 121 includes conductive elements 123 which are received by respective ones of conductive elements 114 when connector 120 is connected to package 110. Similarly, coupling surface 122 includes 25 conductive elements 124 which are received by respective ones of conductive elements 114 when connector 120 is connected to package 110.

Connector 120 is coupled to cable 125. In some embodiments, conductive elements 123 are electrically coupled to respective ones of conductors within upper surface 126 of

cable 125, and conductive elements 124 are electrically coupled to respective ones of conductors within lower surface 127 of cable 125. Accordingly, conductive elements 111 are electrically coupled to respective ones of conductors within upper surface 126 and other ones of conductive elements 111 are electrically coupled to respective ones of conductors within lower surface 127.

FIG. 4 is a cut-away view of cable 125 according to some embodiments. Shown are upper surface 126 and lower surface 127. Upper surface 126 includes a set of conductors 130 and lower surface 127 includes a set of conductors 135. Conductors 130 may be formed as copper striplines within dielectric substrate 140. Similarly, conductors 130 may be formed as copper striplines within dielectric substrate 145. Middle conductor 150 is sandwiched between substrate 140 and substrate 145 so as to be electrically isolated from conductors 130 and conductors 135. Middle conductor 150 may also comprise copper or any other suitable materials. Conductors 130, 135 and 140 need not be fabricated from identical or similar materials.

Each of conductors 130 is electrically couplable to respective ones of conductive pads 111. In particular, each of conductors 130 is couplable to respective ones of conductive elements 123, which are couplable to respective ones of conductive elements 114, which are electrically coupled to respective ones of conductive pads 111. Similarly, each of conductors 135 is electrically couplable to respective other ones of conductive pads 111 via conductive elements 124 and conductive elements 116.

Housing 160 provides a protective covering for the other components of cable 125. Housing 160 may also physically couple conductors 130 to conductors 135 while electrically isolating conductors 130 and conductors 135 from one another.

FIG. 5 illustrates a system according to some embodiments. System 200 includes system 100 of FIG. 1, memory 300 and motherboard 400. System 200 may comprise components of a desktop computing platform. Memory 300 may comprise any type of memory for storing data, such as a Single Data Rate Random Access Memory, a Double Data Rate Random Access Memory, or a Programmable Read Only Memory.

Memory 300 and motherboard 400 may be electrically coupled to package 110 of system 100. More particularly, motherboard 400 may comprise a memory bus (not shown) coupled to cable 125 and to memory 300. In operation, motherboard 400 may route input/output signals to cable 125 for transmission to conductive pads 111 and may route 5 power and ground signals to pins 118.

The several embodiments described herein are solely for the purpose of illustration. In some embodiments, one or more instances of cable 125 are connected to a single side of package 110 using one or more instances of connector 120. Moreover, one or more of the four sides of package 110 may be connected to at least one cable 125 according to some 10 embodiments. Some embodiments do not require a one-to-one relationship between conductive pads 111 and conductive pads 114, between conductive pads 111 and conductive pads 116, between conductive pads 114 and conductive pads 123, between conductive pads 116 and conductive pads 124, between conductive pads 123 and conductors 130, and between conductive pads 124 and conductors 135. Some embodiments may include any 15 currently or hereafter-known versions of the elements described herein. Therefore, persons skilled in the art will recognize from this description that other embodiments may be practiced with various modifications and alterations.